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(71) Applicant: SYMBIOS, INC. [US/US]; 2001 Danfield Court, Fort Collins, CO 80525 (US).

(72) Inventor: BARTLETT, Donald, M.; 2421 Sunburst Drive, Fort Collins, CO 80525 (US).

(74) Agent: LUCENTE, David, K.; Symbios, Inc., 2001 Danfield Court, Fort Collins, CO 80525 (US).

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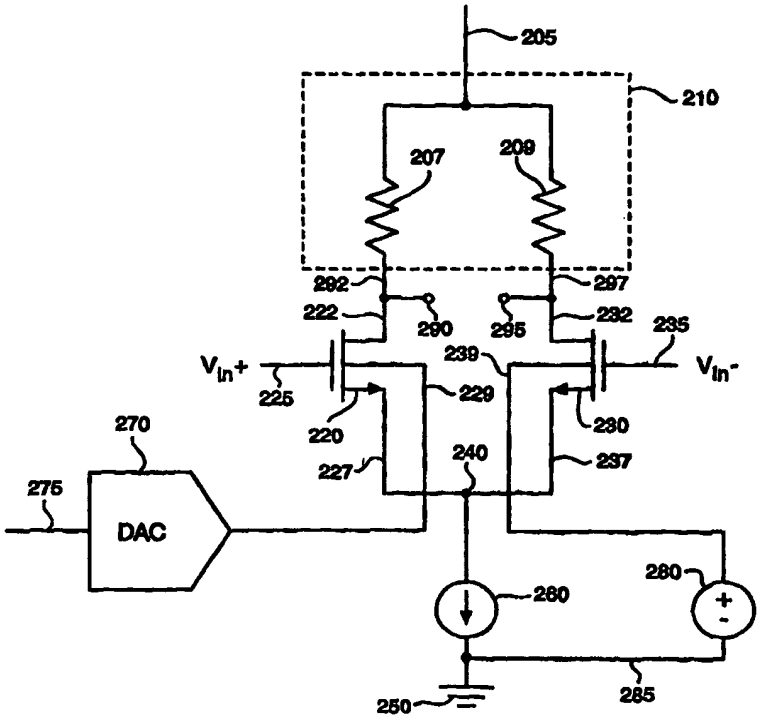
(54) Title: OFFSET ADJUSTMENT OF CMOS MATCHED PAIRS WITH BODY VOLTAGE

(57) Abstract

The present invention includes a method for reducing an offset voltage for transistors (220, 230). The method independently biases a substrate of one of the transistors (220) so that the threshold voltages of the transistors change. This change causes the gate-to-source voltage to change, which can be used to reduce the offset voltage. The biasing includes providing an adjustable bias voltage, such as provided by a digital-to-analog converter (270). The method further includes biasing a substrate of the other transistor (230). The offset voltage is measured at the gates of the transistors (220, 230). Once determined, the adjustable voltage is adjusted to maximally reduce the offset voltage.



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OFFSET ADJUSTMENT OF CMOS MATCHED PAIRS WITH BODY VOLTAGE

1. Field of the Invention

The present invention relates to transistors and more particularly to adjusting the threshold voltage of the transistors.

2. Background of the Invention

Often times two transistors are required to perform the same function, which is termed "matching" of the transistors. To illustrate, FIGURE 1 is an input stage differential amplifier that has matched transistors 110 and 120 coupled to an amplifier load 130. As shown, amplifier load 130 includes resistors 140 and 150. Note that body or substrate connection 135 is connected to ground.

In operation, if transistors 110 and 120 receive $V_{in}+ = V_{in}-$, then the voltage difference between terminals 160 and 170 will ideally equal 0V. However, due to variances between transistors 110 and 120 of the gate conductor material, the gate insulation material, the gate insulator thickness/channel doping, the impurities at the silicon-insulator interface, the voltage between the source and the substrate, or the operating temperature, the voltage difference between terminals 160 and 170 will not equal 0V. This non-zero difference can be represented as the amplified signal $K(V_{in}+ - V_{in}- + V_{offset})$, where V_{offset} is known as an input offset voltage and K is the gain value. This type of amplified signal is undesirable for many analog circuits.

Note that the amplified signal $K(V_{in}+ - V_{in}- + V_{offset})$ at terminals 160 and 170 is caused by the respective drain-source currents I_{ds} through transistors 110 and 120. Drain-source currents I_{ds} can be defined as $I_{ds} = F(V_{gs}, V_t)$, where V_{gs} is the gate-to-source voltage and V_t is the threshold voltage. Thus, adjusting either V_{gs} or V_t will adjust the drain-source current I_{ds} through transistors 110 and 120 to modulate the input offset voltage V_{offset}.

The input offset voltage developed between matched pairs of transistors can be caused by small perturbations in the processing of the two transistors even though the transistors are physically very close to each other on the IC. Input offset voltage of

matched MOS transistors is usually dominated by two factors: threshold voltage mismatch and gate area mismatch.

The threshold voltage V_t of a MOS transistor is a function of the voltage between the source and the substrate of the MOS transistor. This is known as the "body effect." The equation for the threshold voltage V_t that takes into account the body effect is:

$$V_t = V_{t0} + \gamma (2\varphi + |V_{sb}|)^{1/2} - 2\varphi^{1/2} \quad (1).$$

Vt0 is the intrinsic threshold voltage of the MOS transistor when $V_{sb}=0$, γ is the constant that describes the body effect and depends upon the physical properties of the MOS transistor, φ is the Fermi level potential and V_{sb} is the source-to-body or substrate bias voltage. From Equation 1, when $V_{sb}=0$ the threshold voltage V_t equals the intrinsic threshold voltage V_{t0}. Further, as the substrate bias voltage V_{sb} is varied, the threshold voltage V_t changes.

The offset voltage V_{offset} can be described as:

$$V_{offset} = V_{gs110} - V_{gs120} \quad (2),$$

and

$$= V_{t110} + ((2I_{d1}/\mu C_{ox110}(W_{110}/L_{110}))^{1/2} - V_{t120} + ((2I_{d2}/\mu C_{ox120}(W_{120}/L_{120}))^{1/2} \quad (3).$$

Vgs is the gate-to-source voltage, V_{t110} is the threshold voltage of transistor 110, V_{t120} is the threshold voltage of transistor 120, I_{d1} is the drain current of transistor 110, I_{d2} is the drain current of transistor 120, μ is the mobility of the channel for both transistors 110 and 120 (this parameter is determined by the silicon process), C_{ox} is the capacitance of the gate oxide per area, W is the physical drawn width of transistors 110 and 120, and L is the physical drawn length of transistors 110 and 120.

If each of the parameters in Equation 3 match, $V_{offset} = 0$. However, because of limitations in the accuracy of the physical dimensions of fabricated transistors, impurities within the material of the transistors or a mismatch in devices in amplifier load 130, $V_{offset} \neq 0$. One way to trim the offset voltage V_{offset} is by physically trimming the load devices in amplifier load 130. This can be accomplished by trimming resistors in amplifier load 130 with a laser. However, this method is intrusive, not accurate and once made, the device cannot be adjusted again when in the field.

Consequently, a need exists for a device that provides a transistor pair with a reduced offset voltage, particularly over the life span of the transistor pair. The present invention meets this need.

3. Summary of the Invention

The present invention includes a method for reducing an offset voltage for transistors. The method independently biases a substrate of one of the transistors so that the threshold voltages of the transistors change. This change causes the gate-to-source voltage to change, which can be used to reduce the offset voltage. The biasing includes providing an adjustable bias voltage, such as provided by a digital-to-analog converter. The method further includes biasing a substrate of the other transistor. The offset voltage is measured at the gates of the transistors and, once determined, the adjustable bias voltage is adjusted to maximally reduce the offset voltage.

Numerous other advantages and features of the present invention will become readily apparent from the following detailed description of the invention and the embodiments thereof, from the claims and from the accompanying drawings in which details of the invention are fully and completely disclosed as a part of this specification.

4. Brief Description of the Drawings

In the drawings,

FIGURE 1 is a diagram of an amplifier with a load; and

FIGURE 2 is a diagram of an amplifier with a load incorporating an embodiment of the present invention.

5. Detailed Description of the Preferred Embodiment

While this invention is susceptible of embodiment in many different forms, there is shown in the drawings and will be described herein in detail a specific embodiment thereof with the understanding that the present disclosure is to be considered as an exemplification of the principles of the invention and is not to be limited to the specific embodiment described.

Referring to Equation 3 above, each of the parameters can be termed as the difference of that parameter between matched transistors. For example, the difference in drain currents I_d for transistors 110 and 120 is:

$$\Delta I_d = I_{d110} - I_{d120}.$$

Using this approach to define the other parameter changes in equation 3, and assuming the use of resistive devices in amplifier load 130, the expression $V_{gs110} - V_{gs120}$ can be rewritten as:

$$\Delta V_{gs} = V_{offset} = \Delta V_t + (V_{gs} - V_t)/2[(-\Delta R/R) - (\Delta(W/L)/(W/L))] \quad (4).$$

By creating a difference in the substrate-bias voltage ΔV_{sb}, the threshold voltages V_{t110} and V_{t120} can be made to vary with respect to each other. As a result, varying the threshold voltages V_{t110} and V_{t120} will compensate for any offset voltage V_{offset} due to differences in the other parameters of Equation 4. As will be described below, the present invention utilizes independent control of the substrate-bias voltage V_{sb} to compensate for the input offset voltage V_{offset}.

The present invention will be explained with reference to FIGURE 2. An amplifier load 210 includes resistors 207 and 209, and is coupled to a power supply via a lead 205. Amplifier load 210 is coupled to drains of n-channel transistors 220 and 230 through respective leads 223 and 233. Gates of transistors 220 and 230 are coupled to receive input voltages on respective leads 225 and 235. Sources of transistors 220 and 230 are coupled to a node 240 via respective leads 227 and 237. Node 240 is coupled to another power supply 250 that provides a voltage or ground reference. A current source 260 is provided between node 240 and ground reference 250.

A substrate of transistor 220 is coupled to a digital-to-analog converter (DAC) 270 via a lead 229. DAC 270 is coupled to receive a digital signal on a lead 275. A substrate of transistor 230 is coupled to a voltage supply 280 via a lead 239. Voltage supply 280 is coupled to ground reference 250 via a lead 285. Terminals 290 and 295 are coupled to leads 222 and 232, at nodes 292 and 297, respectively.

The operation of the present invention will be explained with reference to FIGURE 2. Voltage supply 280 preferably provides a positive voltage bias to the substrate of transistor 230 so that DAC 270 will only have to provide a minimal voltage bias of 0V. DAC 270 outputs a voltage on lead 229 in response to the digital signal input. The output voltage of DAC 270 can be adjusted, which in turn will adjust the substrate bias voltage V_{sb} for transistor 220. Thus, the difference between threshold voltages V_t for transistors 210 and 220 can be adjusted, which will cause a change in the drain-source current I_{ds}. By measuring the offset voltage V_{offset} at the gates of transistors

220 and 230, DAC 270 can be adjusted to minimize the offset voltage V_{offset}, preferably to 0V.

The present invention is particularly advantageous in calibrating and re-calibrating a device having matched transistors. To illustrate, when the device is tested after manufacture, DAC 270 can be adjusted to minimize or zero the offset voltage V_{offset}. The device can also be constantly or controllingly re-calibrated while in use. For example, a comparator or an analog-to-digital converter can be coupled to the device shown in FIGURE 2 to monitor the offset voltage V_{offset}. The comparator or ADC can be coupled at either the gates of transistors 220 and 230, or at terminals 290 and 295. The comparator or ADC can then provide a result in digital format to a microprocessor. The microprocessor then can provide signals to DAC 270 to vary the substrate bias voltage of transistor 220 until the offset voltage V_{offset} is reduced to a minimum or zero. The present invention therefore provides the capability of repeated re-calibration of the device over the device's life span.

Numerous variations and modifications of the embodiment described above may be effected without departing from the spirit and scope of the novel features of the invention. For example, DAC 270 can be replaced by any source that provides an adjustable or variable voltage. Such a source can be a programmable resistive device. In addition, voltage supply 280 can provide any voltage, including 0V. Alternatively, voltage supply 280 can be a DAC or other source of a voltage. Another alternative is that the substrate of transistor 230 can be coupled to ground reference 250. It shall be understood that the n-channel transistors 220 and 230 can be replaced by p-channel transistors.

The present invention is particularly advantageous for use with fixed common-mode amplifiers requiring good offset performance. Another use of the present invention is for providing an offset adjustment for transistors having small channel width/length that has poor offset performance, but good frequency response.

It is to be understood that no limitations with respect to the specific device illustrated herein are intended or should be inferred. It is, of course, intended to cover by the appended claims all such modifications as fall within the scope of the claims.

I CLAIM:

1. A method of calibrating transistors comprising the step of biasing a substrate of one of the transistors to reduce the offset voltage.

2. The method of claim 1 wherein the step of biasing biases the substrate of one of the transistors independent of biasing a substrate of another transistor.

3. The method of claim 1 wherein the step of biasing includes providing an adjustable bias voltage.

4. The method of claim 3 wherein the adjustable bias voltage is provided by a digital-to-analog converter.

5. The method of claim 4 wherein a plurality of digital signals are providable to the digital-to-analog converter.

6. The method of claim 1 further comprising the step of biasing a substrate of another transistor.

7. The method of claim 1 wherein the transistors can be re-calibrated.

8. A method of reducing an offset voltage for matched transistors comprising the steps of:

biasing a substrate of a first transistor with a first bias voltage; and

biasing a substrate of a second transistor with a second bias voltage.

9. The method of claim 8 wherein the first bias voltage is constant.

10. The method of claim 8 wherein the second bias voltage is adjustable.

11. A method of reducing an offset voltage for at least two transistors comprising the steps of:

biasing a first transistor substrate with a constant voltage;

biasing a second transistor substrate with an adjustable voltage;

measuring an offset voltage; and

adjusting the adjustable voltage to reduce the offset voltage.

12. A method for reducing an offset voltage of a pair of transistors comprising the step of adjusting a difference between respective substrate bias voltages of the transistors to reduce the offset voltage.

13. An apparatus for reducing an offset voltage for two transistors comprising:

an adjustable voltage supply coupled to a substrate of one of the transistors; and

another voltage supply coupled to a substrate of another one of the transistors.

14. The apparatus of claim 13 wherein the adjustable voltage supply is a digital-to-analog converter.

15. A differential amplifier comprising:

at least two transistors coupled between a node and a load, and coupled to receive respective voltages; and

an adjustable voltage supply coupled to a substrate of a one of the transistors.

16. The amplifier of claim 15 further comprising another voltage supply coupled to another one of the transistors.

17. The amplifier of claim 15 wherein the transistors are coupled in parallel.

18. The amplifier of claim 15 wherein the adjustable voltage supply is a digital-to-analog converter.

FIG. 1

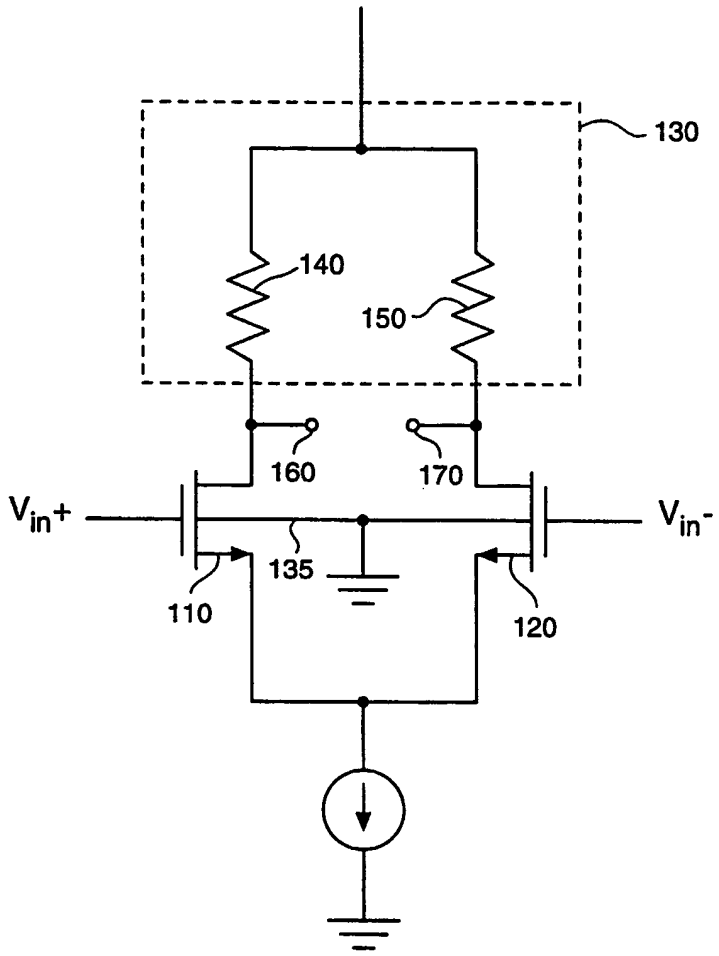
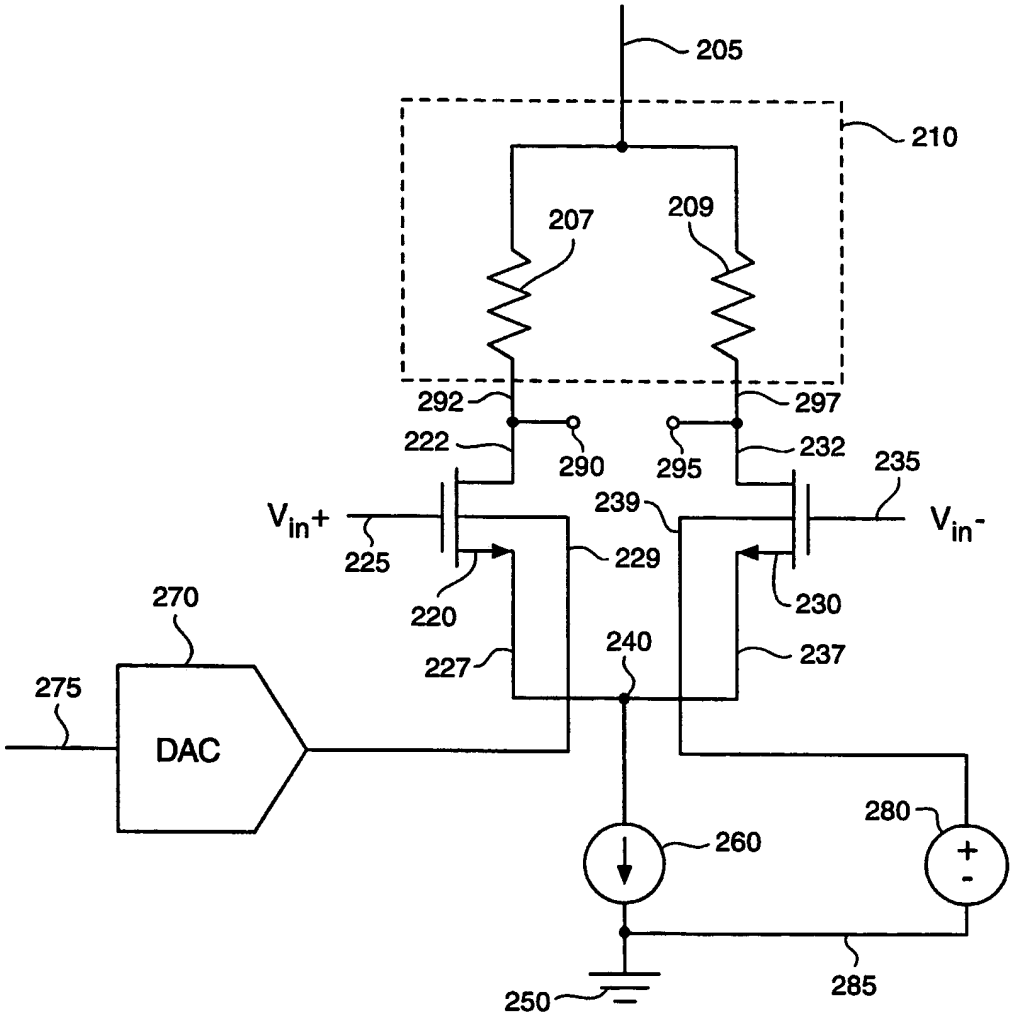


FIG. 2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V_{in}-
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INTERNATIONAL SEARCH REPORT

Inte onal Application No
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A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03F3/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category °	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	H.N. LEIGHTON: "Back Gate Control Circuits" IBM TECHNICAL DISCLOSURE BULLETIN, vol. 27, no. 6, November 1984, pages 3607-3608, XP002086016 NEW YORK US see the whole document	1-18
X	PATENT ABSTRACTS OF JAPAN vol. 096, no. 009, 30 September 1996 & JP 08 125463 A (HITACHI LTD), 17 May 1996 see abstract	1-3,7, 12,15
X	EP 0 367 707 A (IBM) 9 May 1990 see abstract; figures 1,3	1,8,12, 15

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Information on patent family members

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